DESIGN OF QCA BASED ENERGY EFFICIENT ERROR TOLERANT ADDER USING MAJORITY GATE

A. Bhavadharani
PG scholar, *Department of Electronics and Communication Engineering*
Pandian Saraswathi Yadav Engineering College, Sivagngai

Abstract

Integrated circuits have become much smaller, robust and less expensive revolutionizing the electronics world. Over the decades, CMOS have played a crucial role in the integrated circuits. The exponential scaling and increase in processing speed have been provided by CMOS technology for implementing VLSI systems. The present CMOS technology does not sustain the growth levels expected by the semiconductor industry. Nanotechnology is proposed as a solution to the problem because it overcomes the existing power dissipation and also because of the growing demand for denser and faster integrated circuits. Quantum dot-Cellular Automata technology (QCA) emerges as an effective alternative of CMOS-VLSI. Any digital circuit can be implemented by utilizing the QCA-based majority gates. In this work, a approximate adder implemented with quantum-dot cellular automata (QCA) is proposed. The most basic arithmetic operation is the addition of two binary digits, i.e. bits. In many fields the adder plays an important role but in most of the field the accuracy is not in concern. So we proposed a novel approximate adder of quantum dot cell automata (QCA). The proposed adder is used to reduce the circuit complexity and time delay with low error rate. The circuit complexity reduction is achieved by reducing the majority gate in the adder circuit. The operation of QCA circuits is simulated and verified using QCA Designer bistable vector simulation

Introduction

The integrated circuit designers are facing new challenges due to the exponential growth in electronic devices and equipment in the past few years. Addition of more functionality along with real time applications demands revolutionary changes in the design process of a chip. Increase in computing requirements onto a single chip demands development of sophisticated tools that canper form complex operations which further results in increase in the processing power. Thus, development of high-speed computational hardware i.e., adders and multipliers, is a prime concern in today's scenario. For low power and real time applications, computationally intensive digital signal processing algorithms are implemented in dedicated VLSI systems.

In recent years, the use of CMOS technology is limited by high consumption, low speed, and density beyond 10 nm. To overcome these problems, a number of researchers have been ascertained to find the solution for this classical CMOS technology which is quantum-dot cellular automata (QCA) used for high-speed application.

Recently, using QCA technology for electronic modules design has become widely used. The memory circuits have been proposed. The reversible full adder/subtractor and multiplier has been designed. A sequential circuit based on QCA technology has been proposed. A decoder circuit based on QCA technology has been developed.

Sanchez-Macian et al analyzed the effect of QCA majority gate defects in the processing of images when using approximate adders. This is done by evaluating the variation in common error distance metrics in the presence of defects. Mitigation of these defects by combining approximate and exact adders and selective introduction of fault-tolerant majority gates in different bits is analyzed. Perri et al presented the design of approximate binary adders that very effectively exploit the inherent logic and physical behaviors of the Quantum-dot Cellular Automata technology. With respect to state-of-the-art competitors, the 16-bit architecture, designed as proposed here, exhibits an energy-delay-product and an area occupancy up to ~9 and ~3.7 times lower, respectively, with an accuracy more than 10 times higher.

Bahar et al presented an effective single-layer binary discrete cosine transform (BinDCT). To realize the BinDCT architecture in QCA, we also proposed several associated combinational and sequential logic elements of low complexity. All reported circuit layouts were designed and verified using the QCADesigner tool. Moreover, QCAPro is used to estimate the energy dissipation. All comparative study indicates that the reported designs are superior to previous designs in terms of cell complexity, covered area, and energy dissipation. Zhang et al proposed the design of a one-bit approximate full adder based on majority logic. Furthermore, multi-bit approximate full adders are also proposed and studied; the application of these designs to quantum-dot cellular automata (QCA) is also presented as an example. The designs are evaluated using hardware metrics (including delay and area) as well as error metrics. Aravinth et al discussed an approximate adder implemented with quantum-dot cellular automata (QCA). The most basic arithmetic process is the adding of two binary digits, i.e., bits. In many fields the adder plays an important role but in most of the field the accuracy is not in concern. So proposed a novel approximate adder of quantum dot cellular automata (QCA). The proposed adder is used to reduce the circuit complexity and time delay with low error rate. Perri et al presented the design of approximate binary adders that very effectively exploit the inherent logic and physical behaviors of the Quantum-dot Cellular Automata technology. With respect to state-of-the-art competitors, the 16-bit architecture, designed as proposed here, exhibits an energy-delay-product and an area occupancy up to ~9 and ~3.7 times lower, respectively, with an accuracy more than 10 times higher.

Existing System

In 1993, Craig Lent proposed a new concept called quantum-dot cellular automata (QCA). This emerging technology has made a direct deviation to replace conventional CMOS technology based on silicon. QCA generally uses arrays of coupled quantum dots in order to implement different Boolean logic functions. QCAor quantum-dot cellular automata as its name is pronounced uses the quantum mechanical phenomena for the physical implementation of cellular automata. In the general case, conventional digital technologies require a range of voltages or currents to have logical values, whereas in QCA technology, the position of the electrons givesan idea of the binary values. The advantages of this technology are especially given in terms of speed (range of terahertz), density (50 Gbits/cm2) and in terms of energy or power dissipation (100 W/cm2).

Proposed System

Computation's errors and imprecisions can be tolerated in these applications, while having understandable and beneficial utcomes that are perceptible enough for human realization. Actually, with a reasonable reduction in preciseness, many circuit parameters such as the number of devices, energy consumption, delay and area can be reduced. Accordingly, approximate computing is a successful solution for fast computation in error tolerant applications to reach simpler circuits with more energy efficiency. It is notable that, as a design paradigm, approximate computing can be applied in various design levels of abstraction such as transistor, logic, algorithmic, architecture and software

An approximate adder is a circuit that adds two numbers with a certain degree of error, but with reduced resources compared to a full precision adder. In QCA, an approximate adder is typically designed using a combination of quantum gates, such as CNOT gates, Toffoli gates, and Fredkin gates. The basic idea behind the design of an approximate adder in QCA is to trade off precision for simplicity, resulting in a circuit that is faster and requires fewer resources.

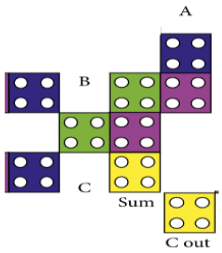

Figure 1 Proposed QCA Adder -2

One approach to designing an approximate adder in QCA involves the use of threshold gates, which are used to represent a range of values. A threshold gate operates by detecting whether the input signal is greater or less than a predefined threshold value. By cascading multiple threshold gates together, it is possible to construct a simple and efficient approximate adder.

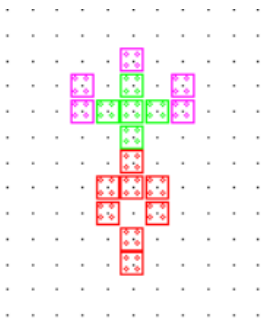

Figure 2 Proposed QCA Adder -1

Table 1 Proposed Adder Truth Table

A	B	C	Carry	sum
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

Results and Discussion

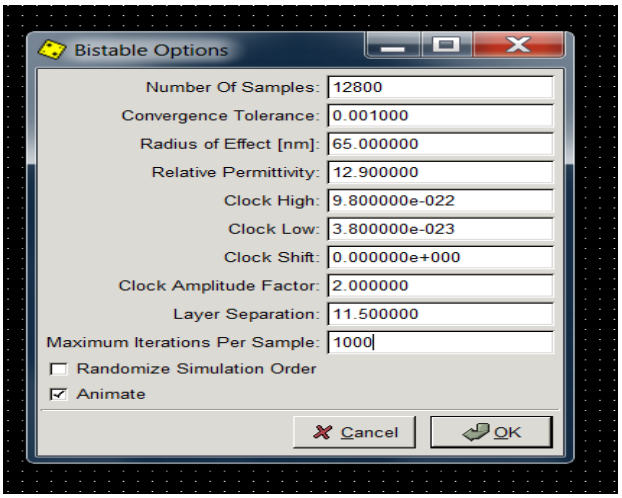

Figure 3 Simulation Parameters

In QCA Designer, can create bi-stable cells by selecting the appropriate option in the Cell Editor and configuring the cell's layout and behavior for approximate adder design as shown in figure 5.1. By using bi-stable cells in your designs, you can create circuits that can store and manipulate digital information, enabling a wide range of computational and communication applications.

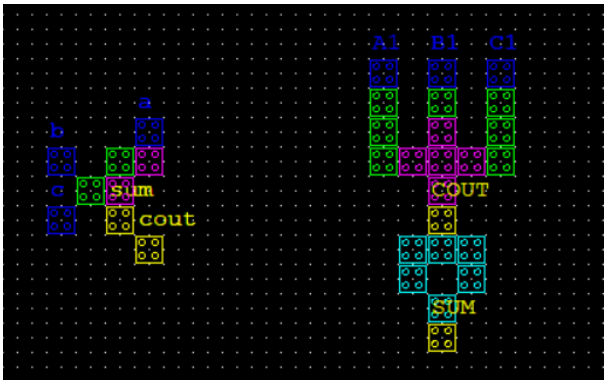

Figure 4 QCA Layout of Proposed Adders

Layout design of adders in QCA involves arranging QCA cells in a specific configuration to implement a desired function or circuit as shown in Figure 5.2. QCA Designer is a software tool that simplifies this process, allowing users to create custom layouts for QCA circuits. To begin the layout design process in QCA Designer.

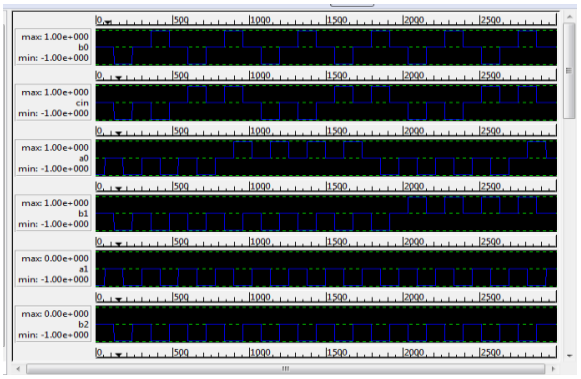

Figure 5 Input Sequence

We can verify input waveforms by simulating your QCA layout design. To verify input and output waveforms, select the "Simulation" tab. By verifying the input and output waveforms in QCA Designer, the layout of proposed design is functioning as intended and refine it as necessary.

Figure 6 Output Sequence

We can verify output waveforms by simulating your QCA layout design. To verify input and output waveforms, select the "Simulation" tab. By verifying the input and output waveforms in QCA Designer, the layout of proposed design is functioning as intended and refine it as necessary.

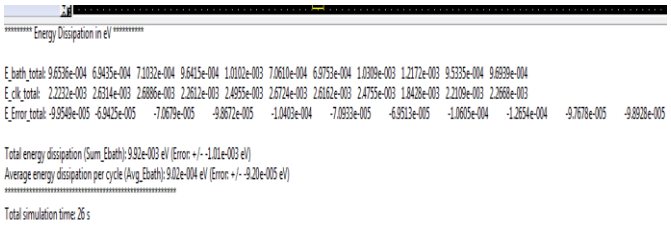

Figure 7 Performance Analysis

Comparison Table

Parameter	Existing	Proposed	Phase-1	Phase -2
Area -Dots	70	46	33	21
Delay -S	55	47	26	12
Energy -J	5.34	2.99	9.20	3.14

Figure 8 Performance Analysis

The number of dots and delay are important factors to consider when designing QCA circuits. In general, a circuit with fewer dots can be advantageous, as it can lead to reduced circuit complexity

and increased speed. The proposed design shows minimum dot requirement and delay in comparison with existing design.

Conclusion

Quantum dot-cellular automata (QCA) emerge as a research area to design nanometer scale logic circuit. In this work, a new QCA based approximate adder's design to perform arithmetic operations is developed. The complete simulation is achieved by different clocking scheme using QCA layout to perform approximate adder operations. The simulation results achieved with minimum cells, area and latency. The comparative study shows reduced delay, latency, power consumption.

References

1. T. Vanaraj, M. Raj and L. Gopalakrishnan, "Energy-Efficient Coplanar Adder and Subtractor in QCA," 2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT), 2020, pp. 539-544, doi: 10.1109/ICSSIT48917.2020.9214274.
2. P. U. Rao and P. Niranjan, "Design of efficient BCD adder with five input majority generators for quantum cellular automata," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), 2020, pp. 1566-1573, doi: 10.1109/ICISS49785.2020.9316010.
3. Z. Chu, Z. Li, Y. Xia, L. Wang and W. Liu, "BCD Adder Designs Based on Three-Input XOR and Majority Gates," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 1942-1946, June 2021, doi: 10.1109/TCSII.2020.3047393.
4. U. B. Joy, S. Chakraborty, S. Tasnim, M. S. Hossain, A. H. Siddique and M. Hasan, "Design of an Area Efficient Quantum Dot Cellular Automata Based Full Adder Cell Having Low Latency," 2021 2nd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST), 2021, pp. 689-693, doi: 10.1109/ICREST51555.2021.9331135
5. K. Swetha, K. L. Krishna, J. V. S. Sowmya, D. S. Reddy, G. Pravallika and G. A. Kumar, "Area Efficient Multilayer Arithmetic Logic Unit Implementation in Quantum-dot Cellular Automata," 2021 Third International Conference on Intelligent Communication Technologies and Virtual Mobile Networks (ICICV), 2021, pp. 584-589, doi: 10.1109/ICICV50876.2021.9388584.
6. S. Perri, F. Spagnolo, F. Frustaci and P. Corsonello, "Accuracy Improved Low-Energy Multi-Bit Approximate Adders in QCA," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 11, pp. 3456-3460, Nov. 2021, doi: 10.1109/TCSII.2021.3077669.